ALPHA DATA

ADM-PCIE-KU3
User Manual

Document Revision: 1.13
20th Dec 2018

	Head Office	US Office
Address:	4 West Silvermills Lane Edinburgh, EH3 5BD, UK	611 Corporate Circle, Suite H Golden, CO 80401
Telephone:	+44 131 558 2600	(303) 954 8768
Fax:	+44 131 558 2700	(866) 820 9956 - toll free
email:	sales@alpha-data.com	sales@alpha-data.com
website:	http://www.alpha-data.com	http://www.alpha-data.com

Table Of Contents

List of Tables

List of Figures

1 Introduction

The ADM-PCIE-KU3 is a high-performance reconfigurable computing card intended for Data Center applications, featuring a Xilinx Kintex UltraScale FPGA.

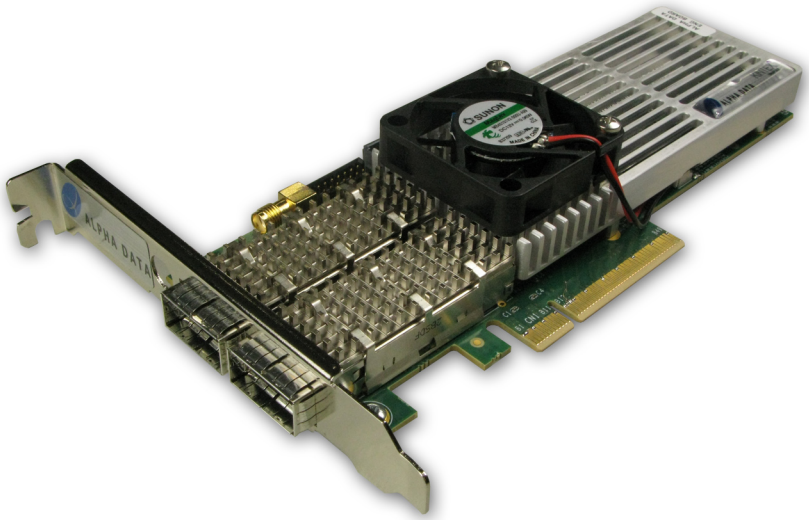

Figure 1 : ADM-PCIE-KU3 Product Photo

1.1 Key Features

Key Features

- PCIe Gen1/2/3 x1/2/4/8/16 capable (x16 requires bifurcation)
- Half-length, low-profile x16 PCIe form factor
- Two banks of DDR3 SDRAM SODIMM memory with ECC, rated at 1600MT/s
- Two right angle SATA connectors (SATA3 capable)
- Two QSFP sites capable of data rates up to 40 Gbps
- SMA timing input
- Front Panel JTAG Access
- FPGA configurable over JTAG and BPI Flash
- XCKU060-2FFVA1156E FPGA
- Voltage, current, and temperature monitoring

1.2 Order Code

ADM-PCIE-KU3/KU060-2E

2 PCB Information

2.1 Physical Specifications

The ADM-PCIE-KU3 complies with PCI Express CEM revision 3.0.

Description	Measure
Total Dy	68.9 mm
Total Dx (Inc. QSFP Cages)	174 mm
Total Dz	32.5 mm
Weight	220g

Table 1 : Mechanical Dimensions

2.2 Chassis Requirements

2.2.1 PCI Express

The ADM-PCIE-KU3 is capable of PCIe Gen 1/2/3 with 1/2/4/8/16 lanes, using the Xilinx Integrated Block for PCI Express.

2.2.2 Mechanical Requirements

A 16-lane physical PCIe slot is required for mechanical compatibility.

Each ADM-PCIE-KU3 is shipped with a full height PCIe card bracket by default. If the application requires a low-profile bracket, contact sales@alpha-data.com before you place your order. Alpha Data will fit the approrpiate bracket to suit either chassis type.

Because most PC chassis do not provide sufficient airflow to cool the FPGA, the ADM-PCIE-KU3 is shipped with a fan on the heatsink. The fan is optional and can be easily removed with a Philips screw driver. The fan consumes part of the adjacent PCIe slot, so the cards must have an unpopulated PCIe slot between them when using the built-in fan. For larger quantities, Alpha-Data can remove the fan prior to shipping. Contact sales@alpha-data.com for details.

2.2.3 Power Requirements

The PCIe Specification permits a standard low-profile, half-length PCIe card to dissipate up to 25 W of power, drawn from the PCIe slot. The ADM-PCIE-KU3 may consume more than 25 W of power for larger user FPGA designs. Power estimation requires the use of the Xilinx XPE spreadsheet and/or a power estimator tool available from Alpha Data. Please contact **support@alpha-data.com** to obtain this tool.

To save power, ensure that QSFP modules are only inserted if used and drive the SODIMMs into power down mode (CKE low and RESET asserted):

2.3 Thermal Performance

The ADM-PCIE-KU3 comes with a heat sink to reduce the heat of the FPGA which is typically the hottest point on the card. The FPGA die temperature must remain under 100 degrees Celsius or the system monitor will clear the FPGA design to ensure the card does not overheat. To calculate the FPGA die temperature, take your application power and multiply by Theta JA from the chart below, and add your systems internal ambient temperature. If you are using the fan provided with the board, you will find Theta JA is approximately 1.38 degC/W for the board in still air.

The power dissipation of the FPGA can be estimated using the Xilinx Power Estimator (XPE) downloadable at http://www.xilinx.com/products/technology/power/xpe.html. Download the UltraScale tool and set the Device to Kintex UltraScale, XCKU060, FFVA1156, -2, Extended. Set the ambient temperature to your system ambient and select User Override for the Effective Theta JA and enter the figure associated with your system LFM in the blank field. Proceed to enter all applicable design elements and utilization in the following spreadsheet tabs. Next acquire the KU3 power esitmator from Alpha Data by contacting support@alpha-data.com. You will then plug in the FPGA power figures along with DDR4 and SFP usage to get an estimated board level power dissipation.

The graph below shows Theta JA of the board with two 3.5 watt QSFP loopback connectors inserted.

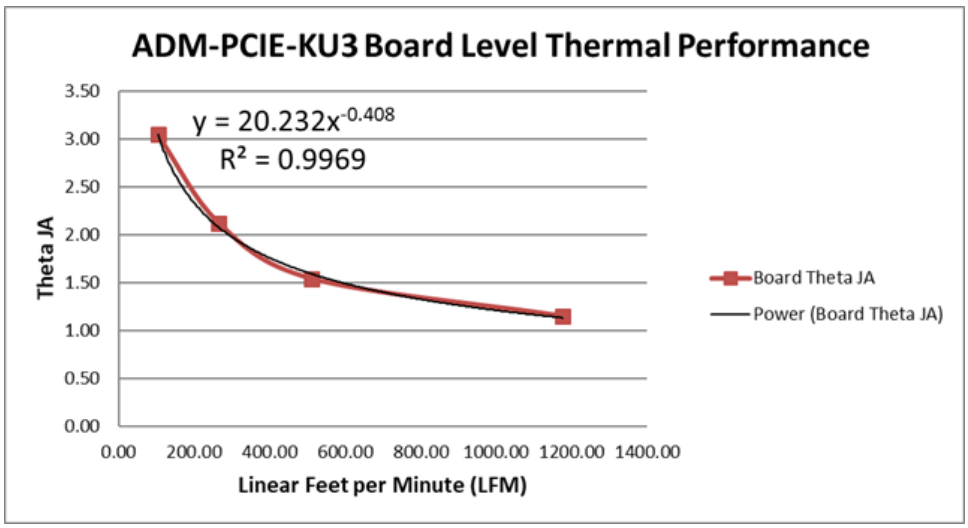

Figure 2 : Thermal Performance

Voltage	Source Name	Current Capability
0.95V	VCC_INT + VCCINT_IO + VCC_BRAM	22A
1.8	VCCAUX + VCCAUX_IO + VCC_BRAM + VCCO_1.8V	3A
3.3	VCCO_3.3V	2.5A
1.5	VCCO_1.5V	7A
1.8	MGTVCCAUX	1A
1.0	MGTAVCC	5A
1.2	MGTAVTT	3A

Table 2 : Available Power By Rail

3 Functional Description

3.1 Overview

The ADM-PCIE-KU3 is a versatile reconfigurable computing platform with a Kintex UltraScale KU040-2E FPGA, two Gen3x8 PCIe interface, two slots for DDR3-1600 SDRAM SODIMMs (64 bits with 8 bits ECC), two QSFP cages capable of 8x 10G or 2x 40G Ethernet, two SATA3 connectors, a SMA input for a timing synchronization input and a robust system monitor.

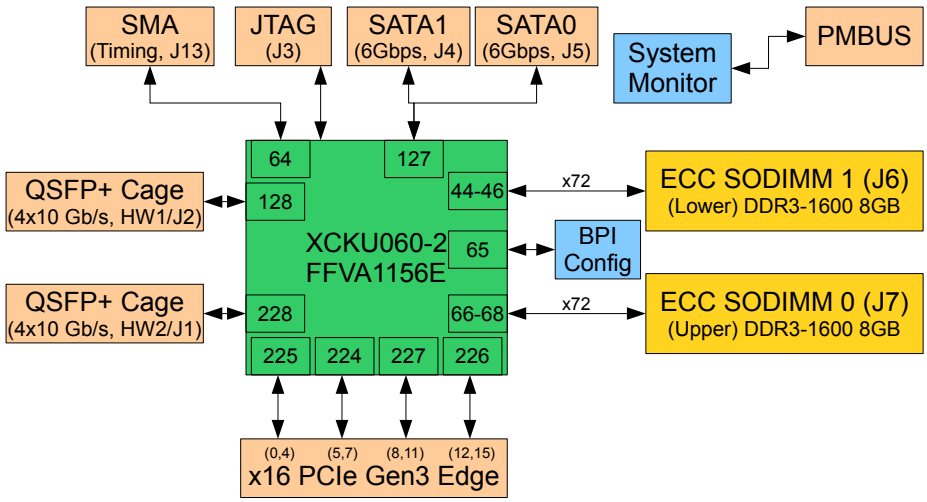

Figure 3 : ADM-PCIE-KU3 Block Diagram

3.1.1 Switches

The ADM-PCIE-KU3 has a quad DIP switch SW1, located on the rear side of the board in the middle of the card along the top edge. The function of each switch in SW1 is detailed below:

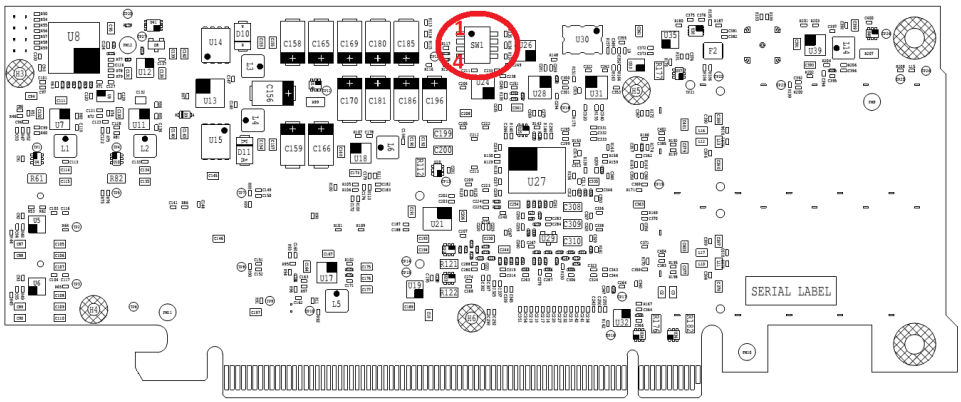

Figure 4 : Switches

Switch	Factory Default	Function	OFF State	ON State
SW1-1	OFF	User Switch	Pin AH12 = '1'	Pin AH12 = '0'
SW1-2	OFF	Flash Lockdown	Flash block Lockdown enabled	Flash block Lockdown disabled
SW1-3	OFF	Xilinx/AD Mode	Configure from Alpha Data region	Configure from Xilinx region
SW1-4	ON	Failsafe/ Default	Configure from failsafe region	Configure from default region

Table 3 : SW1 Switch Functions

Use IO Standard "LVCMOS33" when constraining the user switch pin.

Note:
SW1-1 is also used as a JTAG factory configuration switch when the TI Fusion programing box adapter is plugged into the card. For normal operation of SW1-1 do not use it with the TI Fusion adapter card. If the TI Fusion adapter card is present set SW1-1 ON to communicate with TI tools.

3.1.2 LEDs

There are 7 LEDs on the ADM-PCIE-KU3, 3 of which are general purpose and whose meaning can be defined by the user. The other four have fixed functions described below:

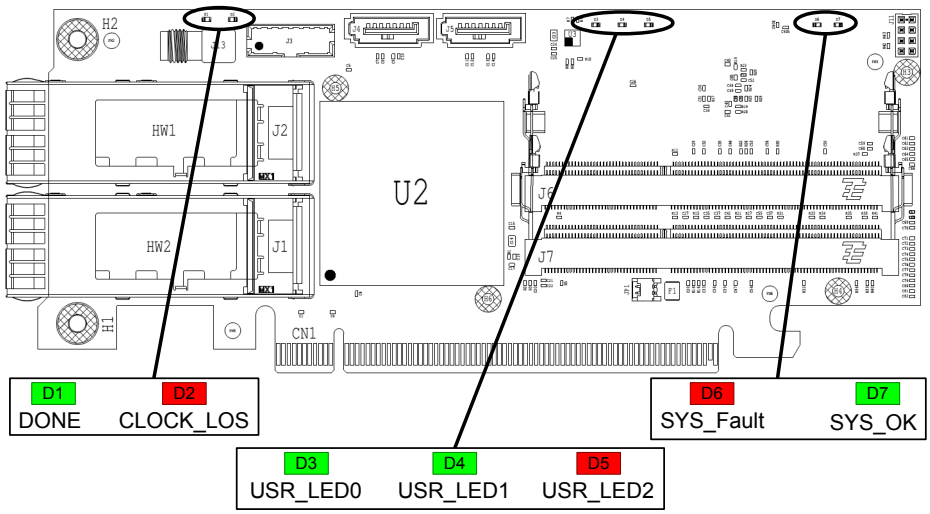

Figure 5 : LEDs

Comp. Ref.	Function	ON State	OFF State
D1	DONE	FPGA is configured	FPGA is not configured
D2	CLOCK_LOS	Clocks not operating normally	Clocks operating normally
D3	USR_LED0	User defined '0' pin AE12	User defined '1' pin AE12
D4	USR_LED1	User defined '0' pin AF12	User defined '1' pin AF12
D5	USR_LED2	User defined '0' pin AD11	User defined '1' pin AD11
D6	SYS_Fault	Temperature or voltage warning/fault	System monitor OK
D7	SYS_OK	Temperature and voltage within tolerance	Temperature or voltage out of tolerance

Table 4 : LED Details

Use IO Standard "LVCMOS33" when driving the user LED pins.

3.2 Clocking

The ADM-PCIE-KU3 provides reference clocks for the DDR3 SDRAM banks and the I/O interfaces available to the user. Any clock out of an Si5338 Clock Synthesizer is re-configurable over I2C. This allows the user to configure almost any arbitrary clock frequencies during application run time. Please contact support@alpha-data.com for details on this process.

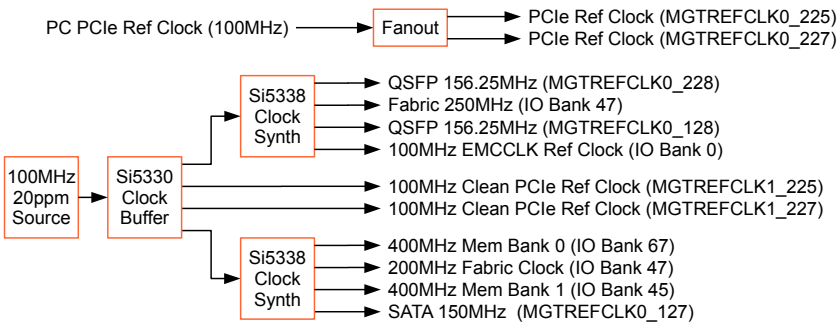

Figure 6 : Clock Topology

3.2.1 PCIe Reference Clocks

The 16 MGT lanes connected to the PCIe card edge use MGT tiles 124 through 127. There are two clocking options available: (i) the internally generated 100 MHz reference clock with a tight 20 ppm tolerance (REFCLK100M_5), and (ii) the system 100 MHz clock (PCIE_REFCLK1).

Signal	Target FPGA Input	I/O Standard	"P" pin	"N" pin
PCIE_REFCLK1	MGTREFCLK0_225	LVDS	AB6	AB5
REFCLK100M_5	MGTREFCLK1_225	LVDS	Y6	Y5
PCIE_REFCLK0	MGTREFCLK0_227	LVDS	P6	P5
REFCLK100M_4	MGTREFCLK1_227	LVDS	M6	M5

Table 5 : PCIe Reference Clocks

3.2.2 Fabric Clocks

The design offers 2 fabric clocks: REFCLK200M is a 200 MHz clock intended to be used for IDELAY elements in FPGA designs. REFCLK250M runs at 250 MHz and can be used to drive internal PLLs and other clocking resources. Each fabric clock is connected to a Global Clock (GC) pin.

Signal	Target FPGA Input	I/O Standard	"P" pin	"N" pin
REFCLK250M	IO_L12P_T1U_GC_47	LVDS	AA24	AA25
REFCLK200M	IO_L13P_T2L_GC_QBC_47	LVDS	W23	W24

Table 6 : Fabric CLocks

Note:
Both fabric clocks are required to be terminated in the FPGA. Use DIFF_TERM_ADV = TERM_100 in the constriant file.

3.2.3 Programming Clock (EMCCLK)

An 100MHz clock is fed into the EMCCLK pin to drive the BPI flash device during configuration of the FPGA.

Signal	Target FPGA Input	I/O Standard	pin
REFCLK100M	IO_L24P_T3U_N10_EMCCLK_65	1V8_CMOS	K20

Table 7 : EMCCLK

3.2.4 QSFP Clocks

The QSFP cages are located in MGT tiles 128 and 228 and use a 156.25MHz reference clock. Note that this clock frequency can be changed to any arbitrary clock frequency up to 400MHz by re-programing the Si5338 reprogrammable clock oscillator via the I2C Interface. Contact supprt@alpha-data.com for more information.

Signal	Target FPGA Input	I/O Standard	"P" pin	"N" pin
REFCLK156M25_1	MGTREFCLK0_128	LVDS	L29	L30
REFCLK156M25_0	MGTREFCLK0_228	LVDS	K6	K5

Table 8 : QSFP and SATA Reference Clocks

3.2.5 SATA Clocks

The two SATA sites are located in MGT tile 227 and share a 150MHz clock.

Signal	Target FPGA Input	I/O Standard	"P" pin	"N" pin
REFCLK150M	MGTREFCLK0_227	LVDS	R29	R30

Table 9 : QSFP and SATA Reference Clocks

3.2.6 DDR3 SDRAM Reference Clocks

The two banks of DDR3 SDRAM memory each require a separate reference clock, as per Xilinx UltraScale MIG design guidelines. The reference clocks for these interfaces are detailed below:

Signal	Target FPGA Input	I/O Standard	"P" pin	"N" pin
REFCLK400M_0	IO_L13P_T2L_GC_QBC_67	HSTL	D23	C23
REFCLK400M_1	IO_L13P_T2L_GC_QBC_45	HSTL	AH18	AH17

Table 10 : Memory Reference Clocks

Note:
Both memory clocks are terminated externally and must not be terminated in the FPGA constraints.

3.2.7 Si5338 Re-programming

The Both Si5338 clock generators are fully reconfigurable. The Alpha Data SDK provides API calls that re-configure certain frequencies with minimal effort. If a user is not using the Alpha Data SDK in their development, they can still change these frequencies manually over an I2C interface. Silicon labs provides detailed descriptions as to how this is done. Please reference the following user guides.

https://www.silabs.com/Support%20Documents/TechnicalDocs/Si5338.pdf

https://www.silabs.com/Support%20Documents/TechnicalDocs/Si5338-RM.pdf

Alpha Data can provide the default register maps of the Si5338 as a starting point. Please contact support@alpha-data.com for these register files.

Both Si5338 devices are on the VPD_SDA/SCL I2C bus (SDA = AG12, SCL = AE11, and LVCMOS33 signaling standard). The upper Si5338 in Clock Topology is at address 0b1110000, while the lower synthesizer is at 0b1110001.

3.3 PCI Express

The ADM-PCIE-KU3 is capable of PCIe Gen 1/2/3 with 1/2/4/8/16 lanes (where 16-lanes requires a two bifurcated 8-lane interfaces). The FPGA drives these lanes directly using the Integrated PCI Express block from Xilinx. Negotiation of PCIe link speed and number of lanes used is generally automatic and does not require user intervention.

PCI Express reset (PERST#) connected to the FPGA at both pins N23 and K22. Do not configure these pins as outputs and do not add a pull-up constraint.

Note:
The Xilinx IP core automatically instantiates a pull-up on PERST#, this MUST be removed for the reset pin to function correctly.

Note:
Different motherboards/backplanes will benefit from different RX equalization schemes within the PCIe IP core provided by Xilinx. Alpha Data recommends using the following setting if a user experiences link errors or training issues with their system: within the IP core generator, change the mode to "Advanced" and open the "GT Settings" tab, change the "form factor driven insertion loss adjustment" to "chip-to-chip".

The other pin assignments for the high speed lanes are provided in the table below:

Signal	Target FPGA Input	P pin	N pin
PCIE_TX0	MGTHTX3_225	AC4	AC3
PCIE_RX0	MGTHRX3_225	AB2	AB1
PCIE_TX1	MGTHTX2_225	AE4	AE3
PCIE_RX1	MGTHRX2_225	AD2	AD1
PCIE_TX2	MGTHTX1_225	AG4	AG3
PCIE_RX2	MGTHRX1_225	AF2	AF1
PCIE_TX3	MGTHTX0_225	AH6	AH5
PCIE_RX3	MGTHRX0_225	AH2	AH1
PCIE_TX4	MGTHTX3_224	AK6	AK5
PCIE_RX4	MGTHRX3_224	AJ4	AJ3
PCIE_TX5	MGTHTX2_224	AL4	AL3
PCIE_RX5	MGTHRX2_224	AK2	AK1
PCIE_TX6	MGTHTX1_224	AM6	AM5
PCIE_RX6	MGTHRX1_224	AM2	AM1
PCIE_TX7	MGTHTX0_224	AN4	AN3
PCIE_RX7	MGTHRX0_224	AP2	AP1
PCIE_TX8	MGTHTX3_227	G4	G3
PCIE_RX8	MGTHRX3_227	F2	F1
PCIE_TX9	MGTHTX2_227	J4	J3

Table 11 : PCI Express Pin Assignments (continued on next page)

Signal	Target FPGA Input	P pin	N pin
PCIE_RX9	MGTHRX2_227	H2	H1
PCIE_TX10	MGTHTX1_227	L4	L3
PCIE_RX10	MGTHRX1_227	K2	K1
PCIE_TX11	MGTHTX0_227	N4	N3
PCIE_RX11	MGTHRX0_227	M2	M1
PCIE_TX12	MGTHTX3_226	R4	R3
PCIE_RX12	MGTHRX3_226	P2	P1
PCIE_TX13	MGTHTX2_226	U4	U3
PCIE_RX13	MGTHRX2_226	T2	T1
PCIE_TX14	MGTHTX1_226	W4	W3
PCIE_RX14	MGTHRX1_226	V2	V1
PCIE_TX15	MGTHTX0_226	AA4	AA3
PCIE_RX15	MGTHRX0_226	Y2	Y1

Table 11 : PCI Express Pin Assignments

3.4 DDR3 SDRAM SODIMMs

Two DDR3 SDRAM SODIMM connectors can accommodate up to two SODIMMs with 72-bit wide data (64 data + 8 ECC). Maximum signaling rate is 1600 MT/s, and maximum memory capacity is 8 GiB per SODIMM. Peak theoretical memory bandwidth for both banks combined is approximately 198 Gbps.

Memory solutions are available from the Xilinx Memory Interface Generator (MIG) tool. An example project and constraint information can be obtained by contacting support@alpha-data.com

3.5 QSFP

Two QSFP cages are available at the front panel. Both cages are capable of housing either active optical or passive copper QSFP compatible components. The communication interface can run at up to 16.375Gbps per channel. There are eight channels between the two QSFP cages (total maximum bandwidth of 131Gbps). These cages are ideally suited for 8x 10G or 2x 40G Ethernet or any other protocol supported by the Xilinx GTH Transceivers. Please see Xilinx User Guide UG576 for more details on the capabilities of the transceivers.

Both QSFP cages have control signals connected to the FPGA. Their connectivity is described in the table below. The I/O standard used by these pins is LVCMOS33.

Signal	iPass Pin	FPGA Pin	|	FPGA Pin	iPass Pin	Signal
QSFP0_SCL	11	AK11	|	AP13	11	QSFP1_SCL
QSFP0_SDA	12	AL13	|	AM11	12	QSFP1_SDA
QSFP0_RESET_L	9	AL12	|	AP11	9	QSFP1_RESET_L
QSFP0_LP_MODE	31	AF13	|	AN13	31	QSFP1_LP_MODE
QSFP0_MODSEL_L	8	GND	|	GND	8	QSFP1_MODSEL_L
QSFP0_INT_L	28	AE13	|	AN11	28	QSFP1_INT_L
QSFP0_MODPRS_L	27	AK13	|	AP10	27	QSFP1_MODPRS_L

Table 12 : QSFP Control Signals

The data path for the two modules is shown in the table below:

Ref. Des.	Signal	Target FPGA Input	P pin	N pin
J2(HW1/UPPER)	QSFP0_TX0	MGTHTX0_128	H31	H32
J2(HW1/UPPER)	QSFP0_RX0	MGTHRX0_128	G33	G34
J2(HW1/UPPER)	QSFP0_TX1	MGTHTX1_128	G29	G30
J2(HW1/UPPER)	QSFP0_RX1	MGTHRX1_128	F31	F32
J2(HW1/UPPER)	QSFP0_TX2	MGTHTX2_128	D31	D32
J2(HW1/UPPER)	QSFP0_RX2	MGTHRX2_128	E33	E34
J2(HW1/UPPER)	QSFP0_TX3	MGTHTX3_128	B31	B32
J2(HW1/UPPER)	QSFP0_RX3	MGTHRX3_128	C33	C34
J1(HW2/LOWER)	QSFP1_TX0	MGTHTX0_228	F6	F5
J1(HW2/LOWER)	QSFP1_RX0	MGTHRX0_228	E4	E3
J1(HW2/LOWER)	QSFP1_TX1	MGTHTX1_228	D6	D5
J1(HW2/LOWER)	QSFP1_RX1	MGTHRX1_228	D2	D1
J1(HW2/LOWER)	QSFP1_TX2	MGTHTX2_228	C4	C3
J1(HW2/LOWER)	QSFP1_RX2	MGTHRX2_228	B2	B1
J1(HW2/LOWER)	QSFP1_TX3	MGTHTX3_228	B6	B5
J1(HW2/LOWER)	QSFP1_RX3	MGTHRX3_228	A4	A3

Table 13 : QSFP Transceiver Signals

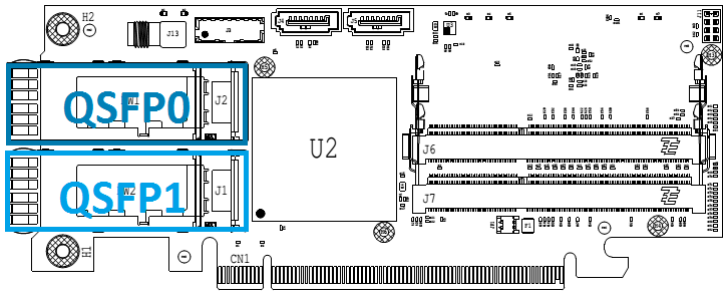

Figure 7 : QSFP Locations

3.6 SATA

Two SATA receptacles along the top of the board allow for internal chassis SATA management. The SATA interface can support the third generation SATA specification operating at 6 Gbps. Alpha Data can provide IP to manage the SATA devices connected at this interface. Please contact sales@alpha-data.com for more information regarding SATA IP.

Both RX and TX lines are AC coupled with 10nF capacitors. The pin assignments for this interface are detailed below:

Ref. Des.	Signal	Target FPGA Input	P pin	N pin
J5	SATA_TX0	MGTHTX0_127	T31	T32
J5	SATA_RX0	MGTHRX0_127	R33	R34
J4	SATA_TX1	MGTHTX1_127	P31	P32
J4	SATA_RX1	MGTHRX1_127	N33	N34

Table 14 : SATA Signals

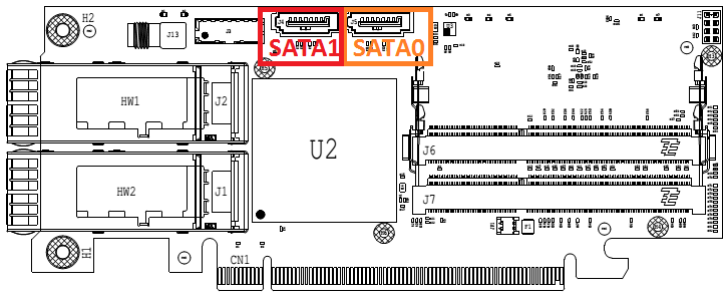

Figure 8 : SATA Locations

3.7 System Monitor

All power rails are sequenced and monitored by a system monitor IC. The device used in this design is a TI Fusion UCD90120A. The TI Fusion controller monitors certain voltage readings, current readings, and Power OK signals to determine the state of the system. D6 and D7 can be decoded to understand the system state (see Section LEDs for LED Location).

LED States	Decoding
Green Only	System status OK
Green and Red	Temperature or voltage warning
Red Only	Currently experiencing temperature or voltage fault

Table 15 : System Monitor LED States

System Monitor Warning Reasons

- FPGA Core Temperature near maximum (95 degC): Warning logged
- Voltage rail outside recommended values in Kintex Ultrascale Datasheet (DS892): Warning logged

System Monitor Faults and Responses

- FPGA Core Temperature above operating above maximum (105 degC): Reconfigure FPGA from failsafe region.
- Voltage rail outside maximums specified Kintex Ultrascale Datasheet (DS892): Power down board.

A PC can directly interact with the TI Fusion IC via the PMBUS header in the design. This requires the following items:

TI Fusion Communication Components

- Programing Box: TI part number "USB-TO-GPIO"
- TI Digital Power Designer software (http://www.ti.com/tool/fusion_digital_power_designer)
- xml configuration file from Alpha Data (contact support@alpha-data.com)
- Alpha-Data program adapter (contact sales@alpha-data.com)

3.8 SMA Timing Input

All cards are fitted with an SMA timing input at the front panel. This can be used to synchronize multiple cards within a system and to timestamp data.

Input is on FPGA pin AG11, IOSTANDARD LVCMOS33

The signal is isolated through a optical isolator part number ACPL-M61L with a 1 Kohm resistor in series.

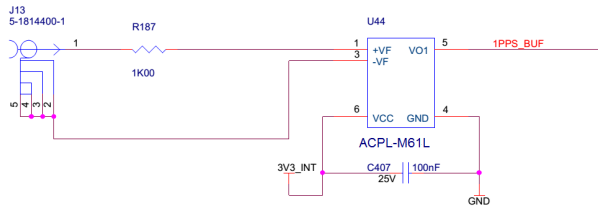

Figure 9 : Timing Input Schematic

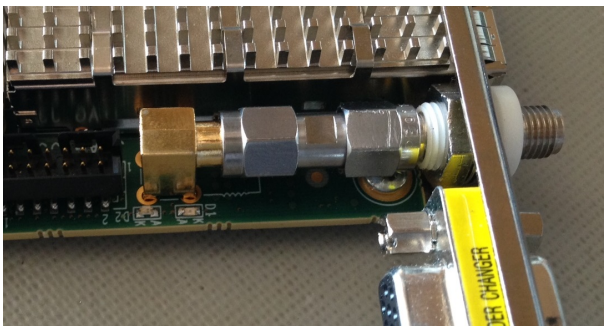

Figure 10 : SMA coupler extender

3.9 JTAG Front Panel Interface

Accessing the JTAG connection for direct configuration of the FPGA can prove problematic if removing the chassis lid is difficult or reduces airflow. To accommodate the need to program the FPGA without access to the JTAG connector on the PCB, a breakout cable can be purchased to bring this connection to the front panel. This item is sold separately. This item is intended to be used in conjunction with the Xilinx Platform Cable USB II.

Alpha Data Part number: contact sales@alpha-data.com

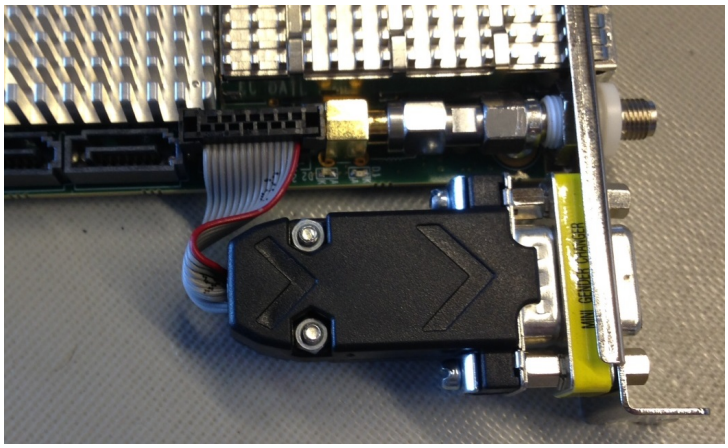

Figure 11 : JTAG cable from PCB to panel

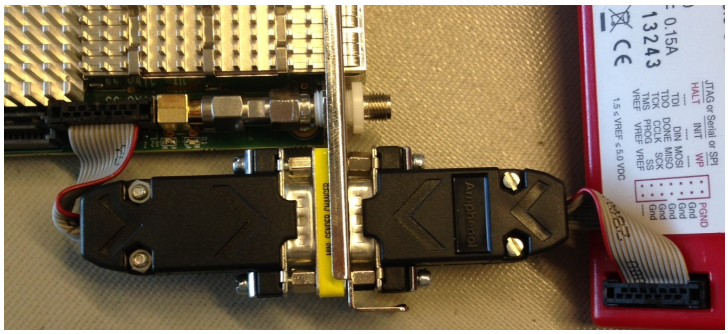

Figure 12 : JTAG cable from panel to Xilinx Platform Cable USB II

3.10 Configuration

There are two main ways of configuring the FPGA on the ADM-PCIE-KU3:

- From Flash memory, at power-on, as described in Section 3.10.1
- Using a Xilinx JTAG platform cable connected to J3, as described in Section 3.10.2

3.10.1 Configuration From Flash Memory

The FPGA can be automatically configured at power-on from a 1 Gbit BPI flash memory device (Micron part number MT28GU01GAAA1EGC-0SIT or PC28F00AG18). This Flash device is divided into four regions of 32 MiByte each, where each region is sufficiently large to hold an uncompressed bitstream for a KU060 FPGA.

The ADM-PCIE-KU3 is shipped with a bitstream, corresponding to the "dma_demo" FPGA design from the ADM-XRC Gen 3 SDK, programmed into region 1 and "reg_access" into region 0. This permits basic confidence testing to be performed on a board without needing to program anything into the Flash memory. Alpha Data recommends that region 0 is never overwritten; this permits relatively simple recovery, without requiring a Xilinx Platform USB JTAG cable to be attached, in the event of programming a "bad" bitstream into region 1.

The flash address map is as detailed below:

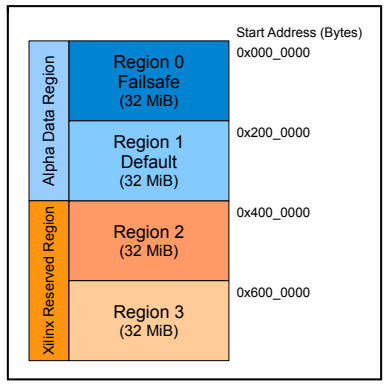

Figure 13 : Flash Address Map

From board revision 4 (s/n 150 onwards), the 2 highest address bits to the flash device are controlled by the FPGA's RS0 and RS1 pins. The setting of SW1-3 and SW1-4 set the pull-up and pull-down on these pins accordingly. If a bitstreams fails to load from flash during the configuration process, the FPGA can use the Failsafe feature to attempt to load a golden image from region 0. For more information on failsafe loads, multiboot, and golden boot, please see Xilinx User guide UG570.

Revision 1,2,3 (S/N 1-149) are set up such that RS1 is not used. Therefore if the SW1-3 is ON, the failsafe function will fall back to region 2, whereas if SW1-3 is OFF, the failsafe function will fall back to region 0.

At power-on, the FPGA attempts to configure itself automatically in BPI mode from one of the four regions of the Flash, determined by SW1-3 and SW-4 (see Section 3.1.1) as follows:

SW1-3	SW1-4	Region used for configuration
OFF	OFF	0
OFF	ON	1 (factory default)
ON	OFF	2
ON	ON	3

Table 16 : Flash Configuration Region Selection

The Lockdown function of the Flash device is controlled via switch SW1-2. When SW1-2 is ON, any blocks in the Flash whose Lockdown flag is set are write-protected. The factory default for the Lockdown flag of all Flash blocks is clear, so that any block in the Flash can be written.

3.10.1.1 Building and Programming Configuration Images

Generate a bitfile with these constraints (see XAPP587):

- set_property BITSTREAM.GENERAL.COMPRESS {TRUE} [current_design]
- set_property BITSTREAM.CONFIG.EXTMASTERCCLK_EN {DIV-1} [current_design]
- set_property BITSTREAM.CONFIG.BPI_SYNC_MODE {TYPE1} [current_design]
- set_property BITSTREAM.CONFIG.UNUSEDPIN {Pullnone} [current_design]
- set_property CONFIG_MODE {BPI16} [current_design]
- set_property CFGBVS GND [current_design]
- set_property CONFIG_VOLTAGE 1.8 [current_design]

Generate an MCS file with these properties (write_cfgmem):

- -format MCS
- -size 128
- -interface BPIx16
- -loadbit "up 0x0000000 <directory/to/file/filename.bit>" (Region0 failsafe location)
- -loadbit "up 0x1000000 <directory/to/file/filename.bit>" (Region1 default location)

Program with vivado hardware manager with these settings:

- BPI part number: mt28gu01gaax1e-bpi-x16
- State of non-config mem I/O pins: Pull-none
- RS bits: 25:24

3.10.2 Configuration via JTAG

A Xilinx Platform USB Cable may be attached to connector J3. This permits the FPGA to be reconfigured using the Xilinx Vivado Hardware Manager.

Revision History

Date	Revision	Changed By	Nature of Change
15 Dec 2014	1.0	K. Roth	Initial Release
17 Dec 2014	1.1	K. Roth	Updated Product Photo, added section on SMA timing input, added section on JTAG front panel access, updated description of user leds.
4 Feb 2015	1.2	K. Roth	Modified section on SMA timing input (standard), Correct QSFP pin assignment table, Modified Mechanical Requirements sections to regarding front bracket fitting, Added comment about re-programability of clocks to Clocking section.
24 Feb 2015	1.3	K. Roth	Correct PCIe reset signal reference from K20 to K22
22 Sep 2015	1.4	K. Roth	Added thermal performance information,Correct PCIe Pin Assignment table,Changed EMCCLK to 100MHz,Updated SMA input section to opto-isolator
2 Nov 2015	1.5	K. Roth	Corrected SMA Timing input pin location, QSFP information on block diagram
14 Jan 2016	1.6	K. Roth	Updated EMC clock frequency in Clock Topology, added note to PCI Express specifying that PERST must not have a pull-up, removed outdated references to SFP+ and QSFP+, Added note in Switches warning users not to use SW1-1 with TI Fusion box.
16 Jan 2016	1.7	K. Roth	Added note on clocking constraints to Clocking.
16 Jan 2016	1.8	K. Roth	UpdatedConfiguration to properly describe flash failsafe function.
23 Aug 2016	1.9	K. Roth	Updated Configuration From Flash Memory to reference proper initial load bitstreams, modified Switches note to add TI Fusion use settings, corrected clock naming for lower Si5338 in Clock Topology, Added Si5338 Re-programming.
28 Oct 2016	1.10	K. Roth	Updated SATA to reference proper SATA_RX1 pin assignment, added note in PCI Express to recommend different PCIe RX equalization in the event of link issues.
9 Jan 2017	1.11	K. Roth	added Building and Programming Configuration Images, added table Thermal Performance to detail available power per rail.
27 June 2017	1.12	D. Flint	Updated Thermal Performance thermal characteristics with data from more accurate testing.
12 Dec 2018	1.13	K. Roth	Updated Switches default positions in table

Page Intentionally left blank

Address: 4 West Silvermills Lane
Edinburgh, EH3 5BD, UK
Telephone: +44 131 558 2600
Fax: +44 131 558 2700
email: sales@alpha-data.com
website: http://www.alpha-data.com

Address: 611 Corporate Circle, Suite H
Golden, CO 80401
Telephone: (303) 954 8768
Fax: (866) 820 9956 - toll free
email: sales@alpha-data.com
website: http://www.alpha-data.com